AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An apparatus comprising:

a data aligner to receive data, having a first data format of a first byte-length granularity or a second data format of a second byte-length granularity where the first and second byte-length granularities are different, from a data transmission link and to align the data into predefined segments for interim storage, based on storage devices in which each storage device has a single read port and a single write port of a fixed byte length; and

a buffer, formed from the storage devices, to receive aligned data from the data aligner for interim storage and to reassemble data output onto a wider data path, the buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the data path, based on the first or second byte-length granularity of the received data, and process fragmentation of data for alignment onto the data path by storing the fragmentation in a next selected storage device, ~~but in which~~ the buffer to use ~~multiple memory~~ the storage devices in a cyclic manner based on the byte-length granularity of the received data, in which buffering of the received data of different byte-length granularity is achieved using storage devices having ~~a~~ the single read port and ~~a~~ the single write port ~~to write data of predefined segments from the data aligner~~.

2. (currently amended) The apparatus of claim 1, wherein the ~~buffer is~~ storage devices are arranged in arrays ~~formed from the multiple memory storage devices~~.

3. (original) The apparatus of claim 2 further including a command control logic to separate commands from data at an input to the data aligner and to process commands to align the data.

4. (currently amended) The apparatus of claim 3 further comprises a data re-aligner at the buffer output, wherein ~~the buffer includes a number of arrays in which~~ data entry may start in any one of the arrays and an orientation bit or bits is to be used to identify the starting array for re-alignment in the data re-aligner.

5. (original) The apparatus of claim 4 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

6. (original) The apparatus of claim 5 further comprising a data fragment collector to collect fragments of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment.

7. (currently amended) The apparatus of claim ~~4~~ 1 wherein the received data ~~is~~ has the first data format based on SPI-4 protocol or has the second data format based on HyperTransport protocol.

8. (canceled)

9. (currently amended) An integrated circuit comprising:

an interface unit to receive incoming data from a higher frequency data transmission link for use by the integrated circuit, the incoming data having a first data format of a first byte-length granularity or a second data format of a second byte-length granularity where the first and second byte-length granularities are different;

a command control unit to receive incoming data from the interface unit and to separate commands from data to process commands to align the data;

a data aligner to receive incoming data from the interface unit and to align the incoming data into a predefined segment for interim storage, based on storage devices in which each storage device has a single read port and a single write port of a fixed byte length; and

a reassembly buffer, formed from the storage devices, to receive aligned data from the data aligner for interim storage and to reassemble data output onto an internal data path, the reassembly buffer to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path, based on the first or second byte-length granularity of the received data, and process fragmentation of data for alignment onto the internal data path by storing the fragmentation in a next selected storage device, ~~but in which~~ the reassembly buffer to use ~~multiple memory~~ the storage devices in a cyclic manner based on the byte-length granularity of the incoming data, in which buffering of the incoming data of different byte-length granularity is achieved using storage devices having ~~a~~ the single read port and ~~a~~ the single write port ~~to write data of predefined segments from the data aligner~~.

10. (currently amended) The integrated circuit of claim 9, wherein the ~~reassembly buffer is~~ storage devices are arranged in arrays ~~formed from the multiple memory storage devices~~.

11. (currently amended) The integrated circuit of claim 9, wherein the storage devices of the reassembly buffer ~~is~~ are structured having multiple matrices arranged into arrays, in which a width of the individual matrix is determined by the internal data path.

12. (original) The integrated circuit of claim 10 further comprises a data re-aligner at the reassembly buffer output, wherein an orientation bit or bits is generated at the data aligner and sent to the data re-aligner to be used to identify the starting array for re-alignment in the data re-aligner.

13. (original) The integrated circuit of claim 12 further including a meta-data unit to receive meta-data from the command control logic and to use the meta-data to realign the data in the data re-aligner.

14. (original) The integrated circuit of claim 13 further comprising a data fragment collector to collect fragments of data that do not fit into the predefined segment in one clock period and to use the fragment in a next clock period to fit into a next segment.

15. (currently amended) The integrated circuit of claim ~~14 wherein one input decode and routing unit decodes and routes incoming data based on SPI-4 protocol~~ 9 wherein the incoming data has the first data format based on SPI-4 protocol or has the second data format based on HyperTransport protocol.

16. (canceled)

17. (currently amended) A method comprising:

aligning data received from a data transmission link into predefined segments for interim storage, wherein the received data has a first data format of a first byte-length granularity or a second data format of a second byte-length granularity where the first and second byte-length granularities are different; and

buffering aligned data in a buffer for interim storage, in which the buffer is based on selected storage devices, in which each storage device has a single read port and a single write port of a fixed byte length, and the buffering to reassemble data output ~~data~~ onto an internal data path of an integrated circuit, the buffering to allow storage of aligned data in wider format to maintain sufficient bandwidth to account for frequency scaling of received data rate to frequency of the internal data path, based on the first or second byte-length granularity of the received data, and process fragmentation of data for alignment onto the internal data path, but the buffering is achieved through buffer arrays in a cyclic manner based on the byte-length granularity of the incoming data and in which the buffering of the incoming data of different byte-length granularity is achieved using storage devices ~~in which individual array elements uses~~ having the single read port and ~~a~~ the single write port ~~to write data of predefined segments from the aligner~~.

18. (canceled)

19. (currently amended) The method of claim ~~18~~ 17 wherein the buffering allows a data entry to start in any one of the arrays and an orientation bit or bits is used to identify the starting array for aligning and subsequent re-aligning at the output of the buffer.

20. (currently amended) The method of claim 19 wherein the data ~~is~~ has the first data format based on SPI-4 protocol or has the second data format based on HyperTransport protocol.

21. (canceled)